AMENDMENTS TO THE CLAIMS

1. (Previously presented) A system comprising:

a first device arranged on a circuit board; and

a programmable capture device arranged on said circuit board, wherein at least one input pin of said programmable capture device is communicatively coupled to at least one externally-accessible signal pin of said first device such that said programmable capture device captures at least one signal from said first device during testing of said first device.

2. (Original) The system of claim 1 wherein said first device is arranged on a first side of said circuit board, and wherein said programmable capture device is arranged on a side of said circuit board opposite said first side.

3. (Original) The system of claim 2 wherein said programmable capture device comprises pins having an arrangement corresponding to an arrangement of pins of the first device.

4. (Original) The system of claim 3 wherein said first device comprises at least one-thousand signal pins.

5. (Currently amended) The system of claim 1 wherein said programmable capture device has a density of input pins on [[the]] order of signal pins of said first device.

6. (Original) The system of claim 5 wherein said first device comprises at least one-thousand signal pins.

7. (Original) The system of claim 1 wherein said first device comprises an Application-Specific Integrated Circuit (ASIC).

8. (Original) The system of claim 1 wherein said programmable capture device comprises a Field Programmable Gate Array (FPGA).

9. (Original) The system of claim 1 further comprising:

at least one output pin of said programmable capture device communicatively coupled to

an interface for a logic analyzer that is external to said circuit board, wherein said interface is arranged on said circuit board.

10. (Original) The system of claim 9 wherein said testing of said first device comprises testing said first device at its normal operating frequency.

11. (Original) The system of claim 10 wherein said logic analyzer has an operational frequency slower than the normal operating frequency of said first device, and wherein said programmable capture device buffers captured signals from the first device and outputs the captured signals at a frequency supported by the logic analyzer.

12. (Original) The system of claim 11 wherein the programmable capture device parallelizes the captured signals.

13. (Original) The system of claim 10 wherein said logic analyzer has an operational frequency greater than the normal operating frequency of said first device, and wherein said programmable capture device buffers captured signals from the first device and outputs the captured signals at a frequency supported by the logic analyzer.

14. (Original) The system of claim 13 wherein the programmable capture device serializes the captured signals.

15. (Previously presented) A method comprising:

triggering testing of a first device arranged on a circuit board; and

capturing data from an externally-accessible signal pin of said first device during said testing by a separate field-programmable data capture device also arranged on said circuit board.

16. (Original) The method of claim 15 further comprising:

outputting at least a portion of the captured data from the field-programmable data capture device to a logic analyzer arranged external to said circuit board.

17. (Original) The method of claim 15 further comprising:

programming the field-programmable data capture device to capture desired data from the first device.

18. (Original) The method of claim 17 wherein said programming comprises:

programming the field-programmable data capture device while said field-programmable data capture device is arranged on said circuit board.

19. (Original) The method of claim 17 further comprising:

communicatively coupling a control system to said field-programmable data capture device arranged on said circuit board for performing the programming.

20. (Original) The method of claim 17 wherein the programming comprises selecting at least one signal pin of said first device from which data is to be captured by said field-programmable data capture device.

21. (Previously presented) A system comprising:

a first means for performing an operation, wherein said first means is arranged on a circuit board; and

a means external to said first means, arranged on said circuit board, for capturing signals from an externally-accessible pin of said first means during testing of said first means, wherein the capturing means is programmable while arranged on said circuit board.

22. (Original) The system of claim 21 further comprising:

a means, arranged external to said circuit board, for analyzing captured signals of the first means, wherein the analyzing means is communicatively coupled to the capturing means.

23. (Original) The system of claim 21 further comprising:

means, arranged external to said circuit board, for programming the capturing means.

24. (Original) The system of claim 23 wherein the programming comprises selecting at least one signal pin of the first means from which signals are to be captured by the capturing means.

25. (Original) The system of claim 21 wherein the capturing means comprises a plurality of input pins that are each communicatively coupled to a different signal pin of the first

means, and wherein the capturing means is programmable to select at least one of said input pins that is to have its received signals output at an output pin of the capturing means.